## REMARKS

Entry of this Amendment in accordance with the provisions of 37 CFR §1.114, and reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the final Office Action dated June 4, 2003.

Appreciation is expressed to Examiner Rao for his courtesy and helpfulness during a telephone interview conducted between Examiner Rao and the undersigned attorney on September 17, 2003. During the course of this telephone interview, the amendments presented herein were discussed. In particular, the amending of claims 17,18, 20, 22 and 24 was discussed concerning including the limitation that the compression strain produced in the gate insulators decreases interatomic distances in the material to suppress leakage current from flowing through the gate insulators. In considering this, Examiner Rao indicated that, although this might serve to clarify the distinctions of the invention over the cited prior art, it would require further and additional further consideration to determine whether these amendments actually place the claims in condition for allowance. Therefore, Examiner Rao advised the undersigned attorney that it would be necessary to file a RCE in order for these amendments to be considered since such amendments could not be entered after final rejection. Therefore, the present amendment is presented together with the filing of a RCE for purposes of obtaining consideration of these amendments as well as the additional amendments and the new claims presented by this Amendment.

By the present Amendment, independent claims 12, 17, 18, 20, 22 and 24 have each been amended to clarify the invention, as will be discussed below. Also, new claims 25 to 37 have been added to define the invention in a means plus function format.

Briefly, the present invention is directed to various embodiments concerning the construction of a semiconductor device in a manner which will serve to reduce leakage current flowing through a gate insulating film or tunneling current. For example, in the first embodiment shown in Fig. 1 and claimed, for example, in independent claim 17, a gate insulating film is comprised of a material as a main component thereof selected from titanium oxide, zirconium oxide and hafnium oxide. As discussed in the abstract regarding this, the above noted materials selected for this gate insulator are those:

> "in which compressive strain is produced [and which] . . . can suppress leakage current flowing through the gate insulators and has high reliability."

With regard to the compression strain state for the gate insulator, page 25, line 27 et seq. states:

> "A method for confirming the compression strain state of the titanium oxide gate insulator is to determine the interatomic distance between the titanium (Ti) atom and the oxygen (O) atom in titanium oxide by a transmission electron microscope (TEM). When no strain exists, the interatomic distance is 0.196nm on the average. This indicates that when the average value of the interatomic distance is greater than 0.196nm, the rutile type titanium oxide film will be in a tensile strained state, and when the average value of said distance is less than 0.196nm, then said film will be in a compression state."

In other words, placing the gate insulator of this type of material in a state of compression strain serves to decrease the interatomic distance in the material thereby

Reconsideration and allowance of amended independent claims 17, 18, 20 and 24, together with their dependent claims, over the cited prior art to Matsushita (JP 53010283) and Van Dover (USP 6,093,944) is respectfully requested. By the present Amendment, each of these claims has been amended to add the clarifying language that the compression strain in the gate insulating film serves to decrease the interatomic

distance in the material to suppress leakage current from flowing through the gate insulators. As such, it is respectfully submitted that these amended claims clearly define over the arrangement taught in Matsushita, whether taken in combination with Van Dover or considered on its own.

In the Office Action, it is stated that Matsushita teaches gate insulators of a material having the main components selected from titanium oxide, zirconium oxide and hafnium oxide in which a compression strain is produced. Reference is made to the basic abstract of Matsushita as evidence of this. However, it is respectfully submitted that nothing in the basic abstract, or the disclosure of Matsushita, teaches anything about compression strain produced in the gate insulators, and particularly nothing about compression strain for reducing interatomic distance to lessen the flow of leakage current through the gate insulator. Quite to the contrary, the abstract simply states "the dielectric material is stable in composition, and has less strains." It is respectfully submitted that "less strains" does not mean "compression strain." Indeed, it could imply an ideal situation of no strain.

With regard to this, the following translated portion of the right hand lower column, lines 1-4, at the bottom of page 2 through the left hand upper column, lines 1-4 of page 3 of the Japanese text reads as follows:

> "By the way, important thing for performance of the MOS transistor is, in the case of using an insulating film other that SiO2 as the gate, to [illegible] by thermal oxidation. [illegible] stabilization of the insulating film composition, strain, + charge of Na, K, etc. in the film, and the like. Thus, it is necessary that these conditions are sufficiently suitable."

Concerning this, it is well known that the CV properties are significantly influenced by the amount of defects such as pin holes in the film. Specifically, such defects become a passageway for electrons resulting in a decrease in the ability of the

film to store charge. Accordingly, the reference to the dielectric film having less strain in the abstract in Matsushita is apparently directed to the goal of minimizing the number of defects in the film.

Obviously, this is completely different than the purpose of the present invention, clearly defined in the amended independent claim 17, 18, 20 and 24 of introducing a compression strain to the gate insulator material (either titanium oxide, zirconium oxide and hafnium oxide in the case of claim 17 and 24 or titanium oxide in the case of claims 18 and 20) to decrease interatomic distance in the material thereby suppressing leakage current. Matsushita, of course, is completely silent on any such structure or any mention of dealing with this problem by reducing interatomic distances by creating compression strain in the insulating film. Accordingly, reconsideration and allowance of amended independent claims 17, 18, 20 and 24 and their respective dependent claims is respectfully requested.

In particular regard to claims 18-20, as acknowledged in the Office Action on page 4, lines 1 and 2, "Matsushita does not specifically describe or teach the gate insulator film is mainly composed of titanium oxide having a rutile crystal structure." Thus, the Office Action goes on to cite Van Dover for suggesting the use of such titanium oxide. In response, Applicants respectfully note that Van Dover relates to dielectric materials comprising amorphous films of titanium oxide doped with lanthanide rare earth elements as described in column 1, lines 7-16 of the reference. As such, Van Dover gives no teaching or suggestion whatsoever of using either rutile type or anatase type titanium oxide, as required by the present invention. Accordingly, particular consideration and allowance of claims 18 and 20 is respectfully requested.

Reconsideration and allowance of independent claim 19 over the combination of Matsushita and Van Dover is also respectfully requested. Concerning this, claim 19

specifically defines the feature of a gate insulator having titanium oxide as a main component having a rutile crystal structure:

> "Wherein the thermal expansion coefficient of the main component material of said gate electrodes is greater than the linear expansion coefficient of said titanium oxide."

Regarding this limitation, obviously Matsushita fails to teach or suggest anything concerning this since, as noted by the Office Action, Matsushita does not teach titanium oxide at all, let alone titanium oxide having a rutile crystal structure. Similarly, Van Dover fails to teach or suggest a titanium oxide having a rutile crystal structure, as discussed above. In fact, the titanium oxide arrangement with the lanthanide rare earth elements doping is quite different than the claimed titanium oxide having a rutile crystal structure. As such, the analysis set forth on page 5 of the Office Action concerning the difference in thermal expansion coefficients between Van Dover's polysilicon gate and their thermal oxide dielectric is not appropriate since Van Dover is using a different type of titanium oxide film. Accordingly, reconsideration and allowance of independent claim 19 over this combination of references is also respectfully requested.

Reconsideration and allowance of independent claim 22 over the cited references to Matsushita and Van Dover is also respectfully requested. An example of an embodiment reading on claim 22 can be found in Fig. 13, discussed on pages of 29 and 30. Specifically, Fig. 13 shows first and second transistors in a substrate where the resist high gate voltages. In particular, as noted on page 29, lines 17-22, the first MOS transistor 203 uses a high permittivity film as a gate insulator such as that used for the MOS transistors in example one. In particular, this high permittivity material is a material having a main component selected from titanium oxide, zirconium oxide and hafnium oxide, as discussed above concerning claims 17, 18, etc. The MOS transistor

303, on the other hand, is not required to have such high speed operation, but is required "to be resistant to high voltage in the event of application of high voltage to the gate" as discussed on page 29, lines 26-28. Therefore, it is discussed on page 30, lines 1-8:

> "the second MOS transistor formed in the I/O circuitry region has a silicon oxide gate insulator 304a having a thickness of 3 nm or greater. A silicon oxide film of 3 nm or greater. A silicon oxide film of 3 nm or greater thickness is useful for reducing both of DT current and FN current. Thus, the second MOS transistor is resistant to high voltage applied between the gate electrode and the substrate and highly reliable in use as a transistor for I/O circuits."

Claim 22 is particularly directed to such an arrangement and defines that the first MOS transistor has a gate insulator comprised of a high-permittivity material to permit high speed operation. Claim 22 also defines the second MOS transistor having a gate insulator containing silicon oxide as a main component to resist high gate voltages.

It is respectfully submitted that nothing in either Matsushita nor Van Dover teach or suggest this claimed structure. In the Office Action, reference is made to page 438 of Matsushita and Fig. 1 of Van Dover, but it is respectfully submitted that nothing in either of those references teach or suggest the claimed features of the first and the last transistor having the high permittivity material recited to permit high speed operation in conjunction with a second MOS transistor having a silicon oxide gate insulator to resist high gate voltages. Therefore, reconsideration and removal of the rejection of claim 22

Reconsideration and allowance of amended claim 12 and its dependent claims over the references to Matsushita and Van Dover is also respectfully requested. With regard to this, claim 12 can be read on an arrangement such as shown in Fig. 15, for example. As shown in Fig. 15, a gate insulator 104a of an anatase type crystal structure is provided. In conjunction with this, a film 20 with tensile stress is provided to

introduce tensile stress into the channel region 10, is discussed on page 33, line 2 et seq. As set forth on page 33, line 23 through page 34, line 11, the anatase type gate insulating film 104a is utilized to help prevent tunneling current from flowing in this structure. This is also discussed on page 41, line 11 et seq. and stating:

> "Also, even if tensile strain is exerted to the gate insulator, the anatase type band gap can be made greater than the rutile type band gap. This makes it possible to check the rise of tunneling current due to tensile strength and to thereby lessen power consumption of the device."

Claim 12 has been amended to particularly define these features and advantages. Specifically, the claim has been revised to first set forth that the state of strain of the channel region is tensile strain, followed by the limitation:

> "and the main crystal structure of said titanium oxide is anatase to inhibit a rise in tunneling current caused by said tensile strength."

As such, clearly nothing in either Matsushita nor Van Dover teach or suggest this combination of features of a tensile strain in a channel region in conjunction with the use of a anatase type gate insulator to reduce tunneling current that can be caused by this compressive strain. Due to the failure of either of these references to teach or suggest this feature, whether considered alone or in combination, reconsideration and allowance of independent claim 12, as amended, together with its dependent claims 13-16 is earnestly solicited.

With regard to the particular rejection of dependent claim 16 over the combination of Matsushita, Van Dover and USP 6,249,0898 to Lau, it is respectfully submitted that nothing in the Lau reference would teach or suggest the complete modification of Matsushita to arrive at the present claimed invention. As noted above, claim 16 is dependent on claim 12, and includes the above noted limitations concerning the particular construction of the anatase type data insulating film in conjunction with the

channel region containing tensile strength. Lau is simply of general interest for teaching the use of ruthenium oxide for forming a conductor. Nothing in Lau suggests making up for the shortcomings in either Matsushita or Van Dover discussed above concerning the relationship between the channel region having tensile strain and the anatase type gate insulator defined by the parent claim 12. Therefore, reconsideration and allowance of claim 16 over the cited prior art is earnestly solicited.

Reconsideration and allowance of newly submitted claims 25-37 is also respectfully requested. These new claims define the features of the present invention in a means plus function format to further emphasis distinctions of the present invention over the cited prior art. For example, new claim 25 defines:

> "Means for narrowing interatomic distance in the material to suppress leakage current from flowing through the gate insulators."

It is respectfully submitted that nothing in either Matsushita or any of the cited secondary references remotely suggest providing such means for suppressing leakage current by reducing interatomic distance within the oxide forming the gate insulator.

New dependent claim 26 further defines the means in terms of specifying the atoms between which interatomic distance is narrowed. Obviously, the cited prior art certainly gives no suggestion of this specific feature.

New dependent claims 27 and 28 define that the means narrows the interatomic [illegible] compressive strain in the gate insulator. As discussed above, the primary reference to Matsushita only discusses strain generally, and certainly never suggests introducing compressive strain to a gate insulator to narrow interatomic distances to suppress leakage current.

New dependent claims 29-32, like claim 18, define that the gate insulator is comprised of titanium oxide as the main component having a rutile crystal structure. As

recognized in the Office Action, the primary reference to Matsushita fails to teach or suggest this, and nothing in the cited secondary references would suggest the use of this material in a specific combination defined by the respective means plus function parent claims.

Finally, new claims 33-37 add the further feature to the above discussed claims of a means for producing tensile stress in the gate electrode in addition to the claimed means for narrowing the interatomic distance in the gate insulator to suppress leakage current. It is respectfully submitted that nothing in any of the cited references, whether considered alone or in combination, would at all suggest this combination of features.

For the reasons set forth above, reconsideration and allowance of the claims, as amended, is earnestly solicited.

In view of the foregoing, it is respectfully submitted that the above-identified application is in condition for allowance. Favorable consideration and prompt allowance of claims 12-37 are respectfully requested.

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Respectfully submitted,

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